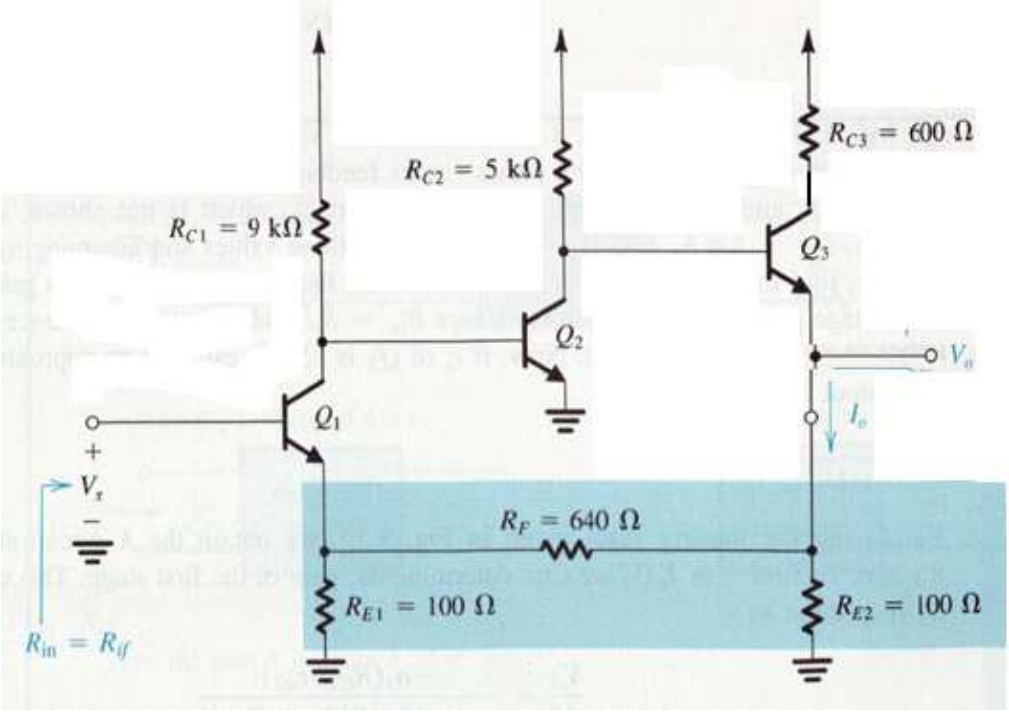
Department
of
Electrical and Computer Engineering, UC.
EE - 352
ELECTRONICS II
SUMMER QUARTER 2010

HOMEWORK ASSIGNMENT #5
Due May 12, 2010



Exercise 8.6. Reconsider the circuit in Fig 8.17(a) (drawn above), this time with the output voltage taken at the emitter of Q3. In this case the feedback can be considered to be of the voltage sampling-series mixing type. Note however that the loop gin remains unchanged. Find the value of $A=V'_{e3}/V'_s$, $A_f=V_{e3}/V_s$ and output resistance.

Data: I_{C1}=0.6mA, I_{C2}=1mA, I_{C3}=4mA, r_{e1}=41.7Ω, $r_{\pi 2}$=2.5kΩ, g_{m2}=40mA/V, r_{e3}=6.25Ω, h_{fe}=100 for all Qs, r_o=oo.

Exersize 8.12. An amplifier with a low frequency gain of 100 and poles at 10^4 and 10^6 rad/s is incorporated in a negative-feedback loop with a feedback factor β. For what value of β do the poles of the closed loop amplifier coincide? What is the corresponding Q of the resulting second order systems? For what value of β is the maximally flat response is achieved? What is the low frequency closed-loop gain in the maximally flat case?

Problem 8.63. An amplifier has a dc gain of 10^5 and poles at 10^5, 3.16×10^5 and 10^6 Hz. Find the value of β and the corresponding closed loop gain for which the phase margin of 45^o obtained.